

REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-7 and 15 are pending in this application. Claims 8-14 are cancelled and Claims 1, 3-6 and 15 are amended by the present response without introducing new matter.

Support for amendments to the Claims can be found in the claims and specification as originally filed. Specifically, support for amendments to Claim 1 can be found in Fig. 1 and page 8, last paragraph.

In the outstanding Office Action, Claims 3-6, 9, 10 and 13-15 were objected to as including informalities; Claims 8-14 were rejected under 35 U.S.C. §101 as directed to non-statutory subject matter; Claims 8-14 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement; Claims 1-7, 9 and 10 were rejected under 35 U.S.C. §112, second paragraph, as indefinite; Claims 1, 2, 4-7 and 15 were rejected under 35 U.S.C. §102(b) as anticipated by Chin et al. (U.S. Pat. No. 5,678,018, herein "Chin"), additionally Ghosh et al. (U.S. Pat. Pub. No. 2002/0069333, herein "Ghosh") is used for inherent teachings; Claim 3 was rejected under 35 U.S.C. 103(a) as unpatentable over Chin in view of Shiell et al. (U.S. Pat. No. 6,442,667, herein "Shiell"); and Claims 8-11, 13 and 14 were rejected under 35 U.S.C. §103(a) as unpatentable over Chin.

In response to the Examiner's request for prior art under §102 or §103, Applicant submits that no such prior art that meets this criteria is known.

In regard to the objection to Claims 3-6, 9, 10 and 13-15, Claims 3-6 and 15 were amended to correct the informalities. Claims 9, 10, 13 and 14 were cancelled and thus the objection to these claims is moot. Accordingly, Applicants respectfully request the objection to Claims 3-6, 9, 10 and 13-15 be withdrawn.

In regard to the rejections under §101 and §112, first paragraph of Claims 8-14, Claims 8-14 were cancelled and thus the rejection of these claims is moot. Accordingly, Applicants respectfully request both the §101 and §112, first paragraph, rejection of Claims 8-14 be withdrawn.

In regard to the rejection of Claims 1-7, 9 and 10 under 35 U.S.C. §112, second paragraph, as indefinite, Claims 1 and 3 have been amended to overcome the rejection. Specifically, Claims 1 and 3 now recite "...based on said signal indicative of cache capacity." Claims 9 and 10 were cancelled and thus the rejection of these claims is moot. Accordingly, Applicants respectfully request the rejection of Claims 1-7, 9 and 10 be withdrawn.

Addressing now the rejection of Claims 11, 2, 4-7 and 15 under 35 U.S.C. §102(b) as anticipated by Chin, that rejection is respectfully traversed.

Claim 1, recites in part,

a bank control circuit, connected to said at least one cache memory, and capable of generating a plurality of control signals for access to said at least one cache memory, said bank control circuit receiving a signal indicative of cache capacity from outside the cache memory device and permitting at least one control signal selected out of said plurality of control signals to access said at least one cache memory, respectively, in accordance with said signal indicative of cache capacity.

Claim 15 recites similar features.

Chin describes a cache memory which adjusts its response to addresses in accordance with the number of identical cache memory cards installed in the motherboard. However, Chin does not describe or suggest that the bank control circuit receives a signal indicative of cache capacity from outside the cache memory device and permits at least one control signal selected out of said plurality of control signals to access said at least one cache memory, respectively, in accordance with said signal indicative of cache capacity.

The outstanding Office Action states on page 8 that “[The bank control circuit] 200 [receives a signal indicative of cache capacity] inherently from the connectors 210 and 212 so the bank control circuit can distinguish whether or not one or two cache memories are installed on the bank control circuit.” In other words, the outstanding Action is stating that the motherboard 200 of Chin is equivalent with the bank control circuit and that the two cache memories 214 and 216 of Chin must inherently sent a signal indicating they exist to the motherboard 200 so that the motherboard 200 can distinguish how many cache memory cards are installed.

However, Claim 1 states that the bank control circuit receiving a signal indicative of cache capacity from outside the cache memory device and permitting at least one control signal selected out of said plurality of control signals to access said at least one cache memory, respectively, in accordance with said signal indicative of cache capacity.

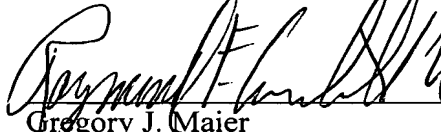
In other words, Claim 1 recites a bank control circuit that receives a cache capacity signal from outside the cache memory device and using this received signal the bank control circuit sends out a control signal to the cache memory. In contrast, when the cache memories 214 and 216 of Chin let the motherboard 200 know they exist the “signal indicative of cache capacity” is not coming from outside the cache memory device.

Therefore, as Chin does not describe or suggest all of the features of Claim 1, Claim 1 and similarly Claim 15 and claim depending therefrom, patentably distinguish over Chin.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-7 and 15 is earnestly solicited.

Respectfully submitted,

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